Microsystem Fabrication Process

Lecture 20

Process Integration

Self-aligned Techniques
- LOCOS self-aligned channel stop
- Lightly Doped Drain (LDD)
- Self-aligned silicide (SALICIDE)
- Self-aligned oxide gap

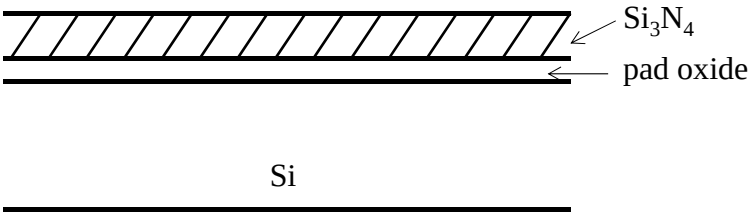
MEMS Release Technique
- Sacrificial Layer Removal
- Substrate Undercut

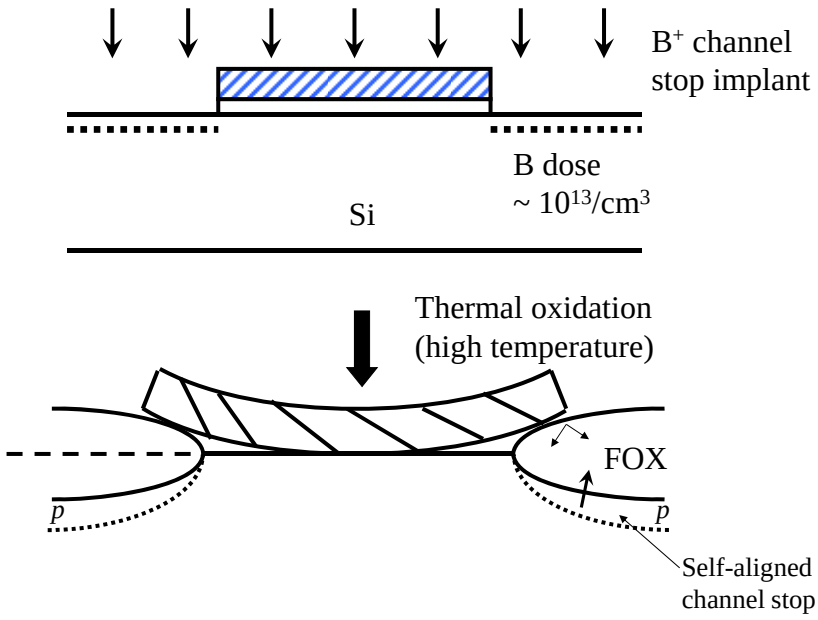
Example IC Process Flows
- NMOS – Generic NMOS Process Flow
- CMOS – The MOSIS Process Flow

Advanced Techniques
- Twin Well CMOS, Retrograde Wells, SOI CMOS

Self-Aligned Channel Stop with Local Oxidation (LOCOS)

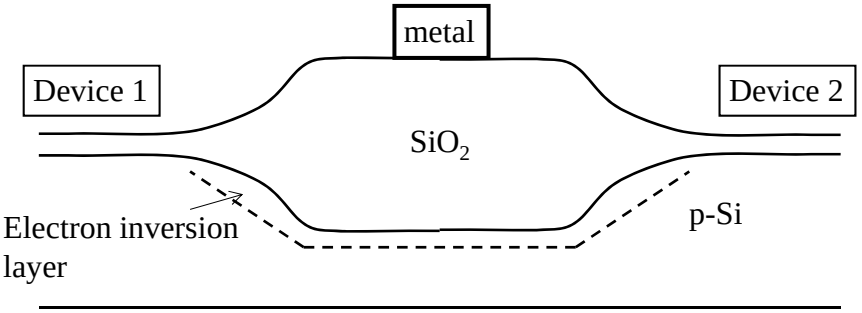
LOCOS Process Flow



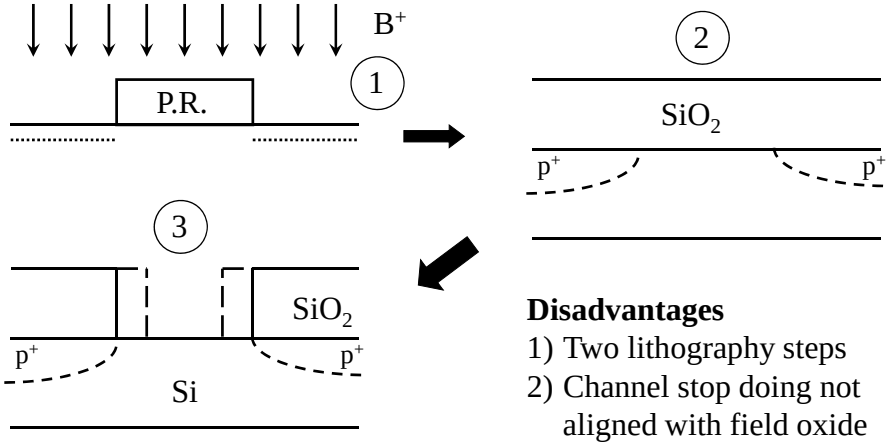


Comment: Channel Inversion

* If a poly or metal line lies on top of the FOX, they will form a parastic MOS structure. If these lines carrying a high voltage, they may create an inversion layer of free electrons at the Si substrate and shorts out neighboring devices. The relatively heavily doped Si underneath (the "channel stop") raises the threshold voltage needed for the inversion.



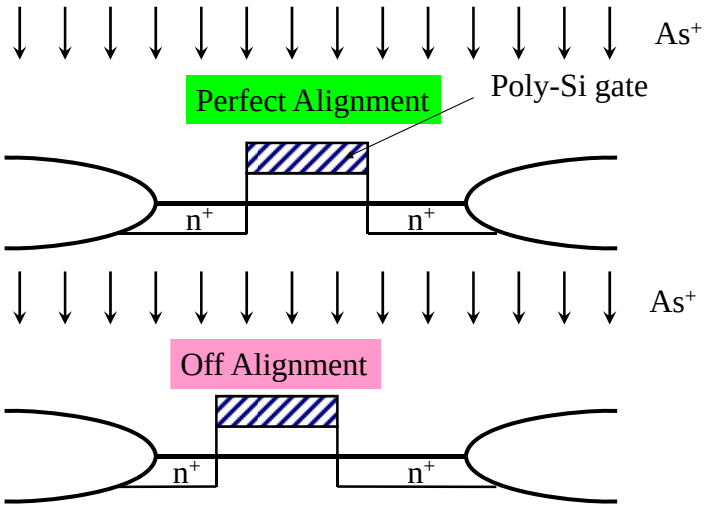
Comments: Non Self-Aligned Alternative



Disadvantages

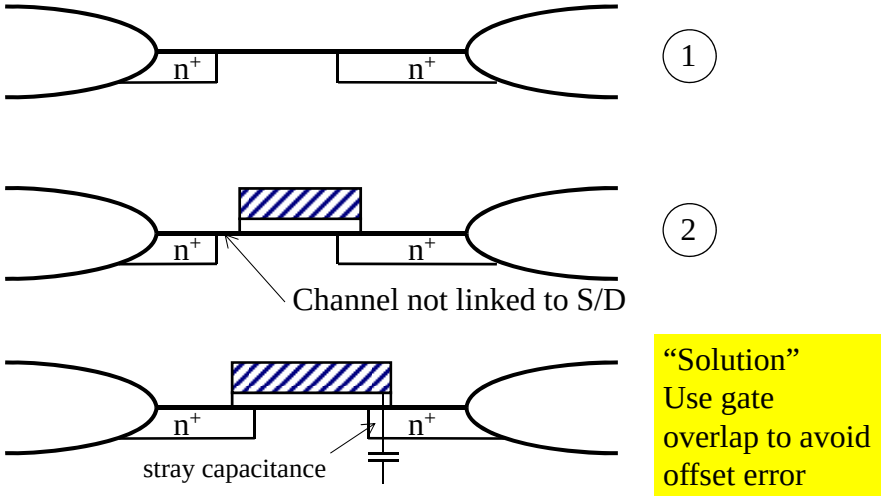
1) Two lithography steps
2) Channel stop doing not aligned with field oxide

Self-Aligned Source and Drain



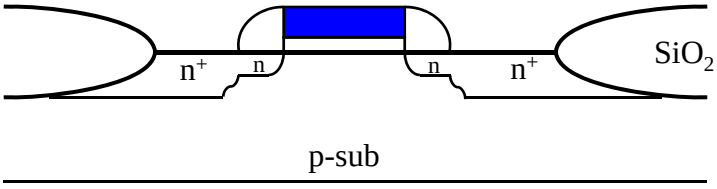
* The n^+ S/D always follows gate

Comment: Non Self-Aligned Alternative



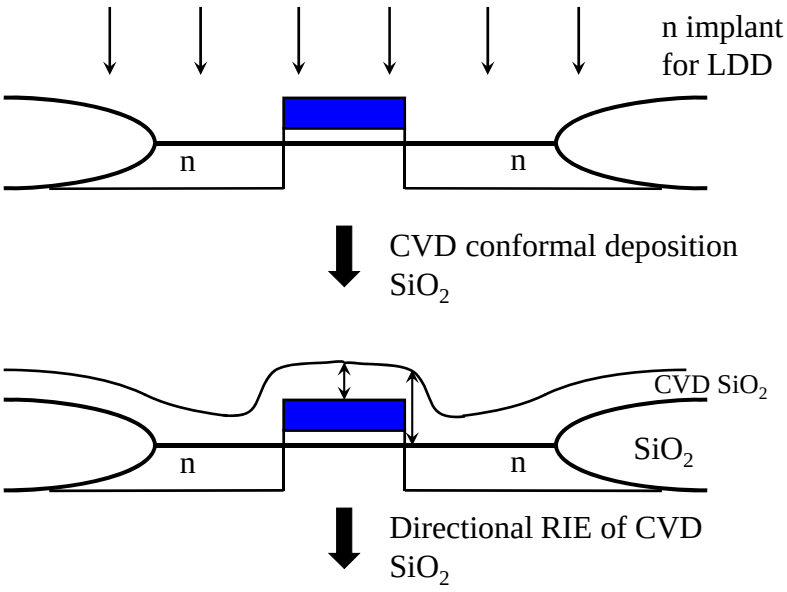
Disadvantage: Two lithography steps, excess gate overlap capacitance

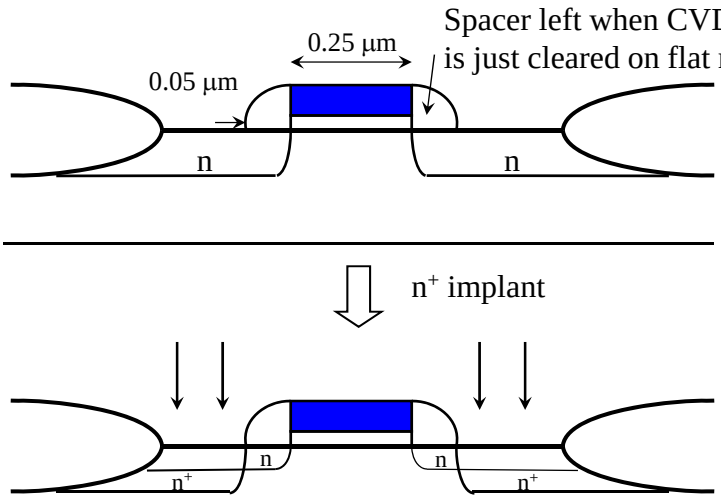
Lightly Doped Source/Drain MOSFET (LDD)



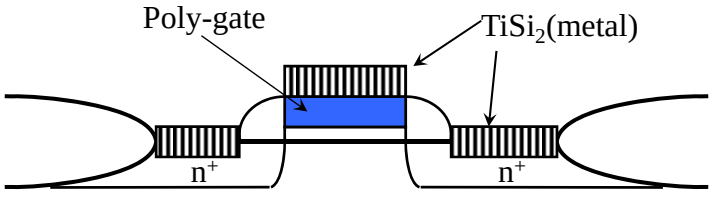
• The n-pockets (LDD) doped to medium concentration (~1E18) is to smear out the strong E-field between the channel and heavily doped n^+ S/D. Less hot-carrier generation.

LDD Process Flow



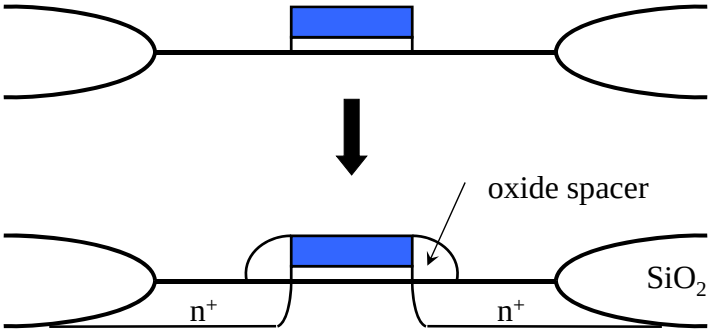


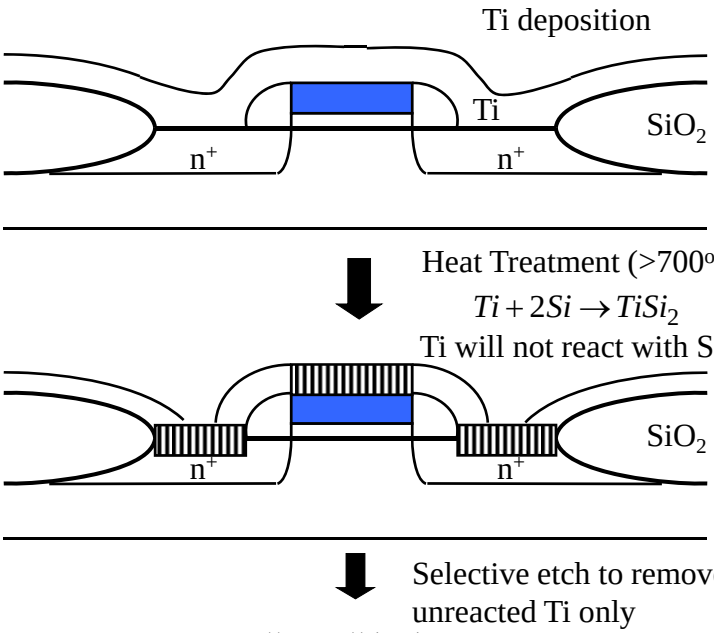
Self-Aligned Silicide Process (SALICIDE)



* Metal silicides are metallics
Lower the sheet resistance of S/D and the poly-gate

SALICIDE Process Flow

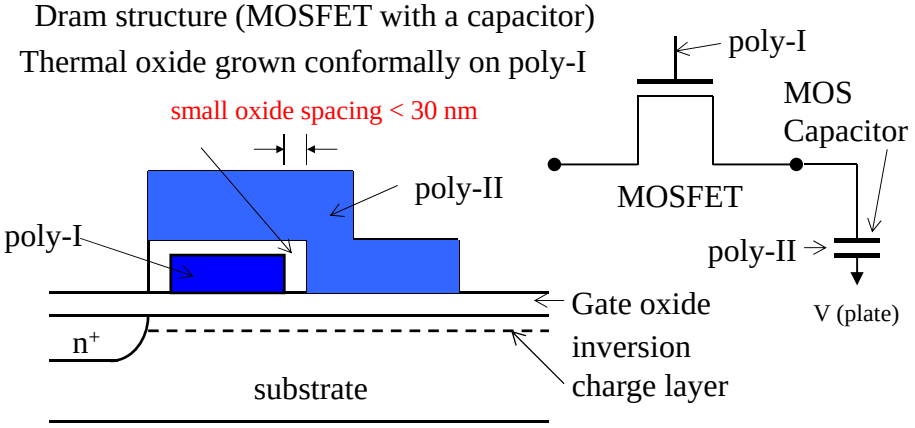




Self-Aligned Oxide Gap

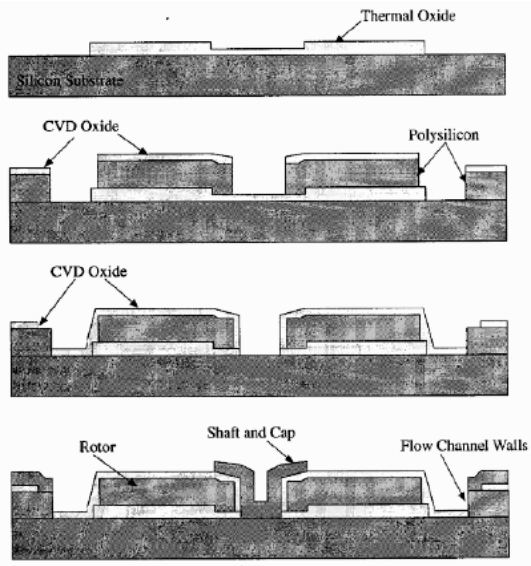
Dram structure (MOSFET with a capacitor)

Thermal oxide grown conformally on poly-I



Note: For a small spacing between poly-I and poly-II, inversion charges between MOSFET and Capacitor are electrically linked. No need for a separate n^+ island.

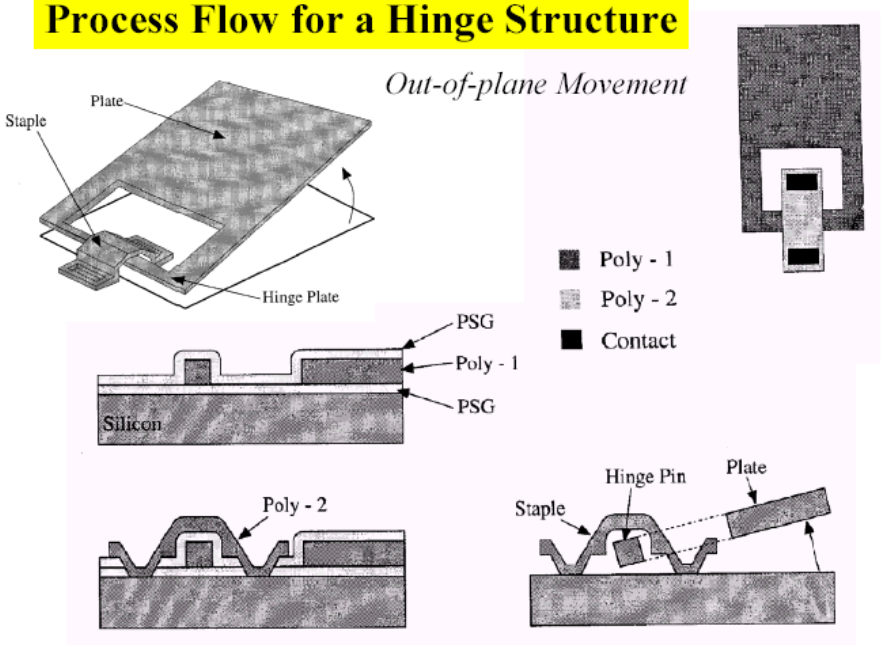
Process Flow of MEMS Rotating Mechanisms



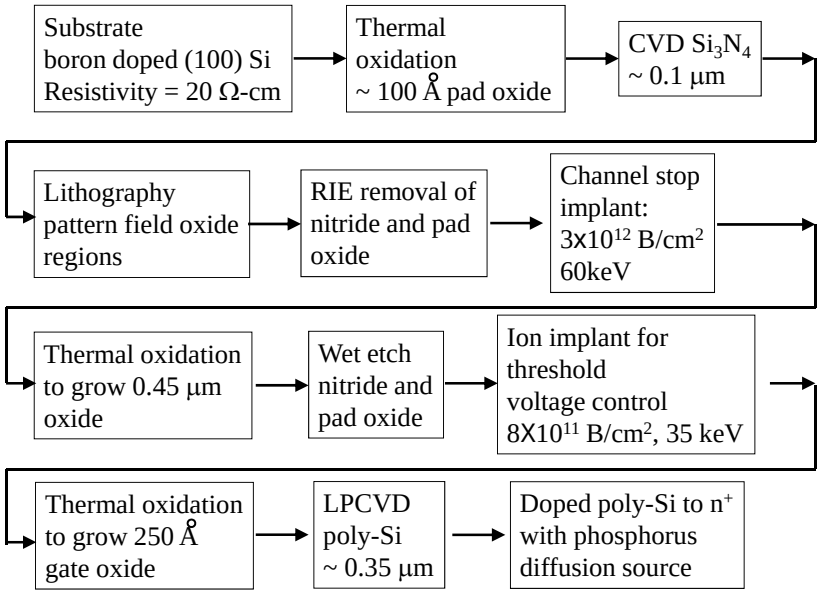
In-plane movement

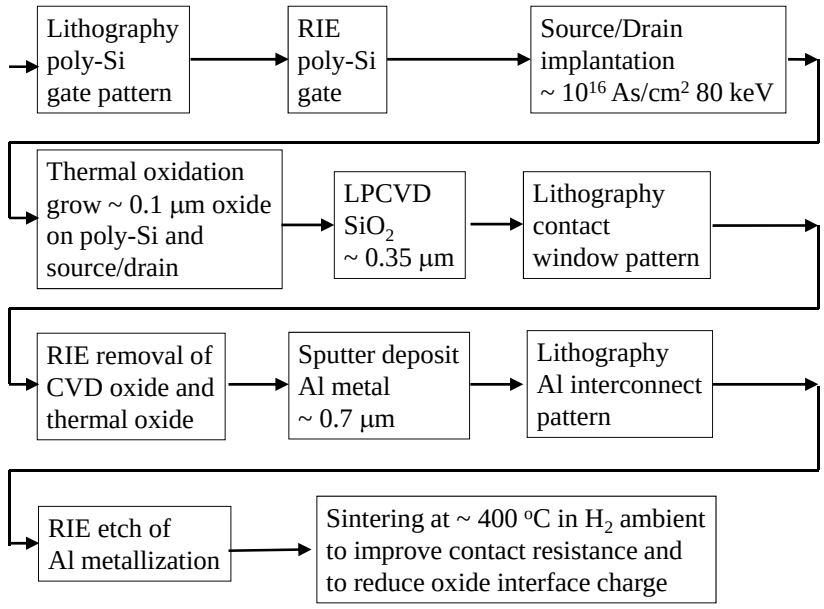
Microturbine Engine

Process Flow for a Hinge Structure

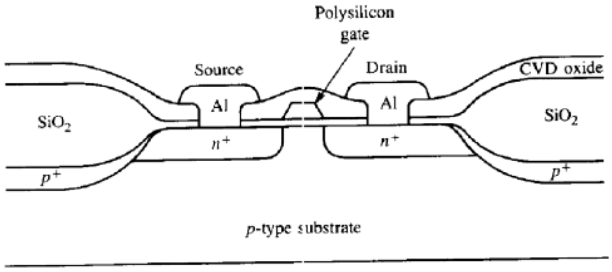


A Generic NMOS Process Flow



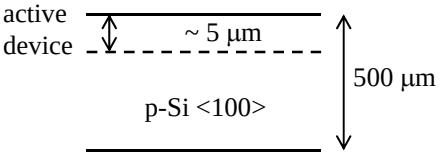


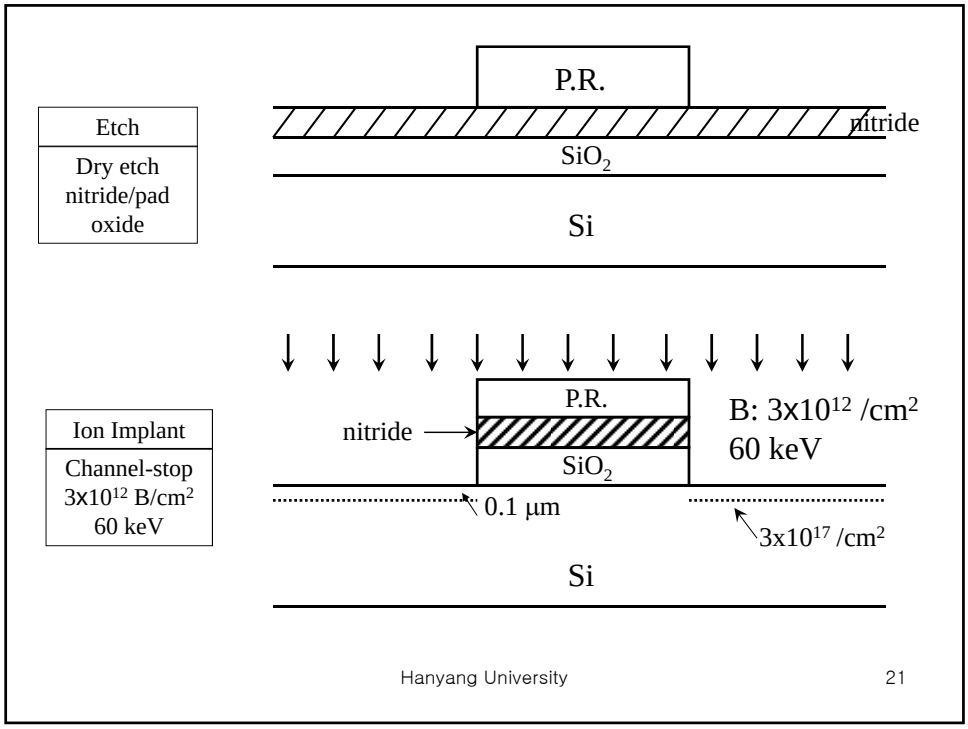
NMOS Structure

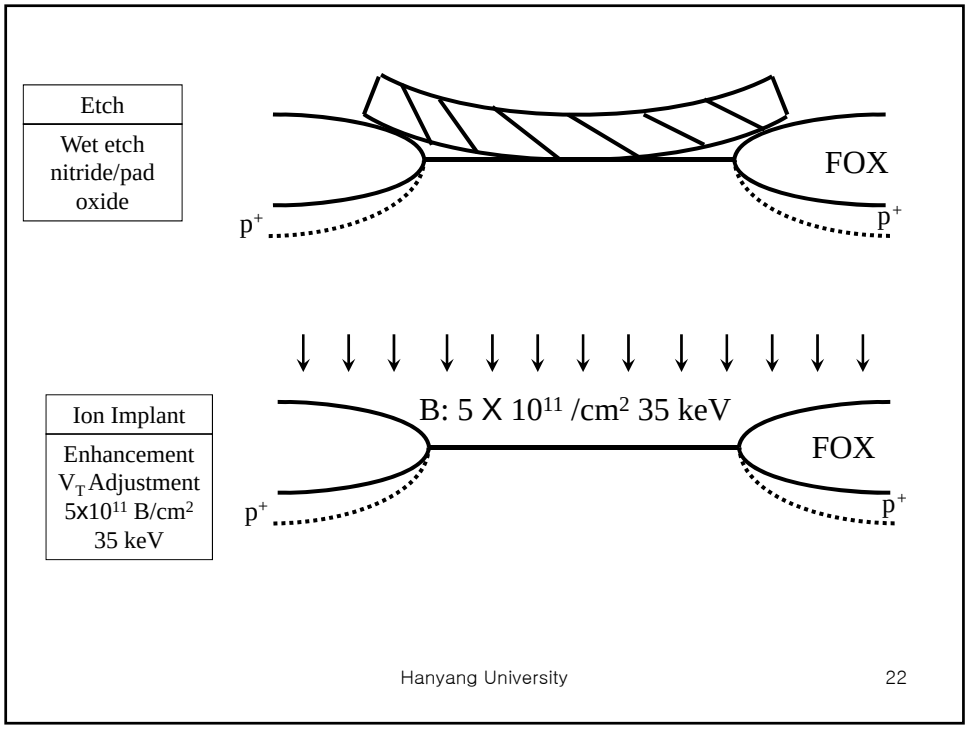


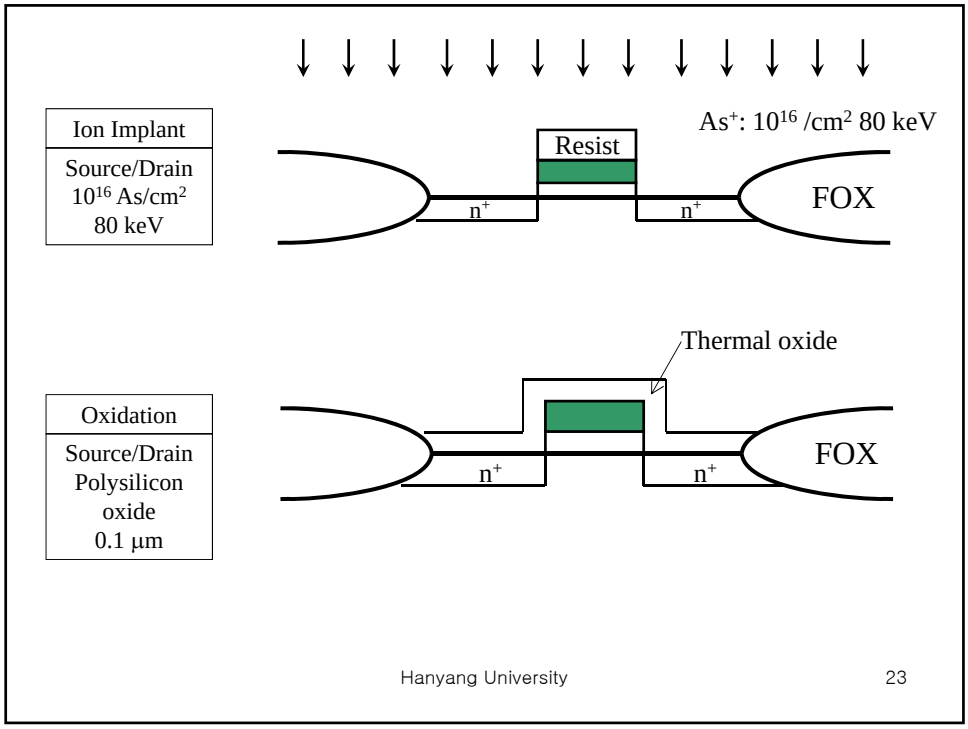
Generic NMOS Process Flow

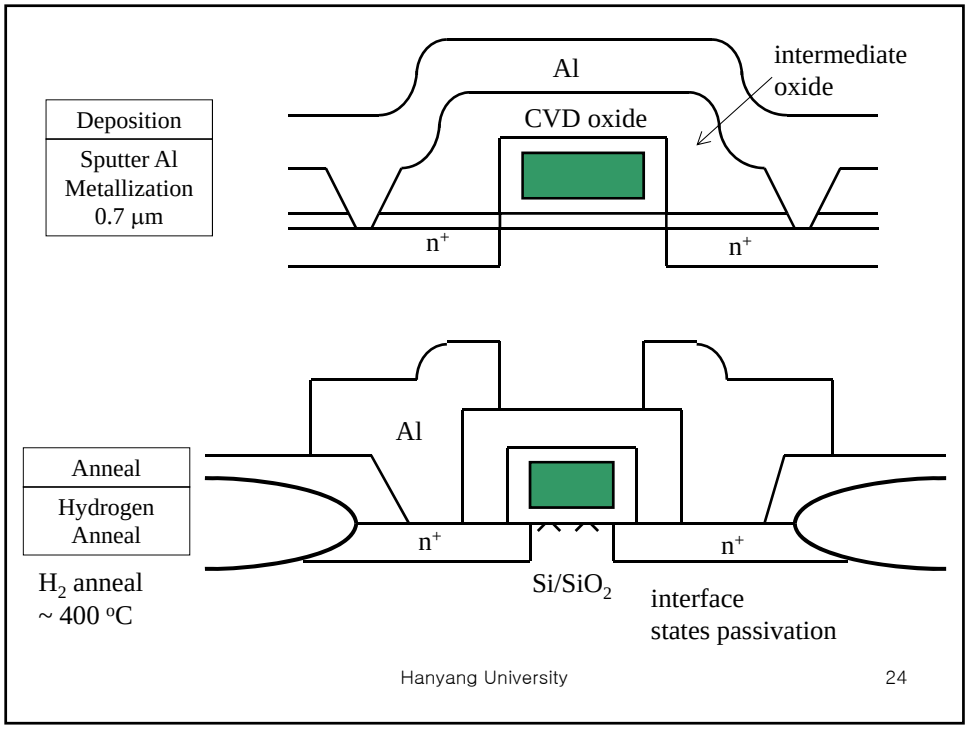
Boron-doped Si
20 Ω-cm
<100>




Etch
Dry etch nitride/pad oxide
P.R.
nitride
SiO2
Si
Ion Implant
Channel-stop 3x10^12 B/cm^2 60 keV
P.R.
nitride
SiO2
B: 3x10^12 /cm^2
60 keV
0.1 μm
3x10^17 /cm^2
Si


Etch
Wet etch nitride/pad oxide
FOX
p+
p+
Ion Implant
Enhancement V_T Adjustment 5x10^11 B/cm^2 35 keV
B: 5 X 10^11 /cm^2 35 keV
FOX
p+
p+


Ion Implant
Source/Drain
10^16 As/cm^2
80 keV
As+: 10^16 /cm^2 80 keV
Resist
n+
n+
FOX
Oxidation
Source/Drain
Polysilicon
oxide
0.1 μm
Thermal oxide
n+
n+
FOX
Hanyang University
23


Deposition
Sputter Al
Metallization
0.7 μm
Al
intermediate
oxide
CVD oxide
n+
n+
Anneal
Hydrogen
Anneal
Al
n+
n+
H2 anneal
~ 400 °C
Si/SiO2
interface
states passivation
Hanyang University
24